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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/816,499

03/23/2001

David G. Ratzel

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07/02/2004

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EXAMINER

LUGO, DAVID B

ART UNIT

PAPER NUMBER

2634

3

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/816,499

Applicant(s)

RATZEL, DAVID G.

Examiner

David B. Lugo

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 14-20 is/are rejected.
- 7) ☒ Claim(s) 4-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed digital phase-locked loop circuit comprising an edge detector, a digitally implemented loop counter, and a digitally implemented phase counter must be shown. It is noted that the only block diagram of a phase-locked loop shown in the figures depicts a prior art circuit. No new matter should be entered.
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: "12" (page 6, line 5), "23" (page 6, line 10).
3. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

In the specification, reference number "30" is used to designate the counter of Figure 4 (page 6, line 19), and the state diagram of figure 5 (page 6, line 29). The specification should be amended such that reference number "30" is used to depict only one of the counter of Fig. 4 and the state diagram of Fig. 5, and the drawings should be amended correspondingly, if necessary.

Appropriate correction is required.

Claim Objections

5. Claims 11-13 and 20 are objected to because of the following informalities:

- a. Claim 11, line 2, "two transitions states" should be --two transition states--.
- b. Claim 12, lines 3-4, "said loop filter" should be --said loop counter--.
- c. Claim 20, line 2, "said phase states" should be --phase states--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hull et al. U.S. Patent 4,808,884.
8. Regarding claim 1, Hull et al. teach a digital phase-locked loop in Figure 9 comprising an edge detector (SYNC 54), a digitally implemented loop counter, considered to include state

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machines 64 and 66, and a digitally implemented phase counter (DCO 60) including variable length shift register 60a, where the transition of the phase counter is responsive to detection of an edge transition in the input bit stream, a transition state of the loop counter, and a prior transition of the phase counter (col. 10, lines 4-43), and the transition state of the loop counter is responsive to detection of an edge transition in the input bit stream, a prior transition state of the loop counter, and a transition state of the phase counter at the edge transition (col. 6, lines 57-68).

9. Regarding claim 2, the clock recovery circuit generates clock pulses (RCLK) on clock line 62 from the inputted data signal (col. 6, lines 20-26).

10. Regarding claim 3, as shown in Figure 10, the digital controlled oscillator controls the shift register to run at different frequencies, where in Figures 10A and 10C, window types of 15 and 17 shift register state durations are utilized, and are considered to include non-linear transitions through the addition or deletion of at least one state. The transition states further include a first set of states indicative of an early phase (up region), and a second set of states indicative of a late phase (down region).

11. Regarding claim 14, the state machines are programmable (col. 4, lines 23-28).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull et al. in view of Cox, Jr. et al. U.S. Patent 4,019,153.

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14. Regarding claim 15, Hull et al. disclose a clock recovery circuit as described above, but do not expressly state that the circuit is part of an integrated circuit. However, implementations of phase-locked loop circuits in integrated circuits are well known in the art. For example, Cox, Jr. et al. disclose a digital phase-locked loop circuit fabricated on a single integrated circuit (col. 3, lines 61-66). It would have been obvious to one of ordinary skill in the art to implement the phase-locked loop circuit of Hull et al. on a single integrated circuit in order enable better performance and reduce space requirements of the circuit.

15. Regarding claim 16, Hull et al. teach a digital phase-locked loop in Figure 9, comprising a digitally implemented phase counter (DCO 60) for indicating a state of the phase counter and enabling a clock output 62 (RCLK), and a digitally implemented loop counter, considered to include state machines 64 and 66, responsive to a phase state of the phase counter (col. 6, lines 57-68), where the phase counter is further responsive to a transition of the loop counter (col. 10, lines 4-43).

16. Hull et al. do not expressly state that the circuit is part of an integrated circuit. However, implementations of phase-locked loop circuits in integrated circuits are well known in the art. For example, Cox, Jr. et al. disclose a digital phase-locked loop circuit fabricated on a single integrated circuit (col. 3, lines 61-66). It would have been obvious to one of ordinary skill in the art to implement the phase-locked loop circuit of Hull et al. on a single integrated circuit in order enable better performance and reduce space requirements of the circuit.

17. Regarding claim 17, the phase counter includes a plurality of registers (variable length shift register 60a) for indicating the transition state of the phase counter (col. 6, lines 14-16).

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18. Regarding claim 18, the loop counter includes a plurality of registers for indicating a transition state (col. 11, lines 8-33).

19. Regarding claim 19, the circuit includes a register (SYNC 54) for indicating detection of an edge of an input bit.

20. Regarding claim 20, the digital controlled oscillator controls the shift register to run at different frequencies, where in Figures 10A and 10C, window types of 15 and 17 shift register state durations are utilized, and are considered to include non-linear transitions through the addition or deletion of at least one state (i.e. Fig. 10A, transition from state 7 to 9).

Allowable Subject Matter

21. Claims 4-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and amended to overcome any objections set forth in this Office action.

22. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to disclose that the loop counter can be in one of a plurality of progressively advancing early phase transition states, a plurality of progressively advancing late phase transition states and a neutral state.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David B. Lugo** whose telephone number is **(703) 305-0954**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

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Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

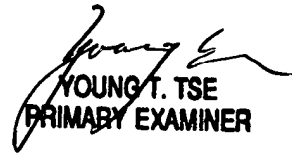
(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dl

6/15/04


YOUNG T. TSE
PRIMARY EXAMINER